Signal Integrity Issues "Past, Present, and Future"

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UltraCAD Design, Inc

PCBs as Components

Signal Integrity Issues related to PCBs.

Stage 1: No Implications

Stage 2: Inductance

Stage 3: R no longer constant with frequency

Stage 4: Transitions and Interconnections
(i.e. "critical length")

Laws

The two most important laws in electronics:

1. **Current flows in a closed loop**
   (This is a physical loop)
2. **Current is constant everywhere in that loop**

Corollary: *Every* signal has a return (no exceptions)
And you need to know where it is!

Other important laws:
Kirchhoff's First Law
Kirchhoff's Second Law
Ohm's Law

Stage Progression (1)

$$V = L * di / dt$$

Noise voltage	Inductance	switched current	**switched time**

Stage Progression (2)

Issue relates to:

Trace propagation time for a signal vs trace length

Frequency (Sine, MHz)	Wavelength (in FR4)
100	59.0 in
200	29.9 in
500	11.8 in
1,000	5.9 in

Rise time	Propagation Distance (FR4)
10 ns	60 in
1.0 ns	6.0 in
100 ps	0.6 in

Stage 1

(Trivial) No signal integrity issues

Stage 2

- **EMI** (caused by inductive loop areas)
- **Crosstalk** (inductive coupling/critical length)
- **Power supply conditioning**
  - (inductively-caused “ground bounce”)
- **Signal Reflections**

  (Rise time < Propagation time)

  (Transmission lines/critical length)

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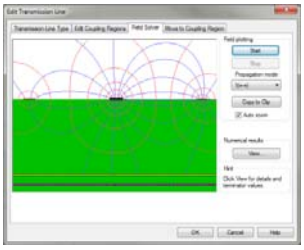
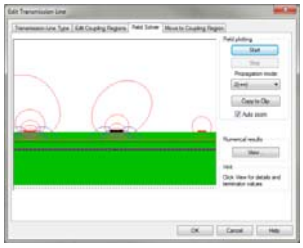
EMI and Crosstalk





Cause: Size of the electromagnetic field is directly related to loop area (and to f^3).

Solution:

1. **Minimize loop area: Route traces close to a continuous, related, underlying plane, and separate the traces.**
2. **Power/Ground planar pairs.**

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EMI and Crosstalk

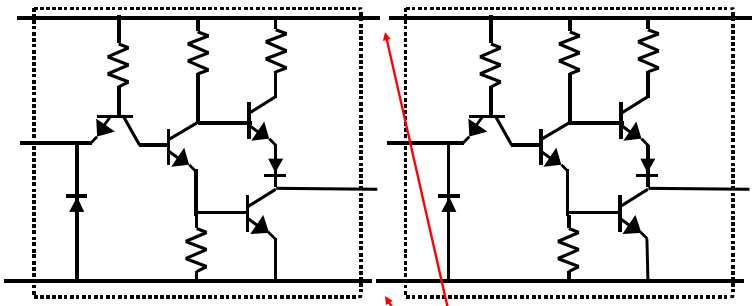
Typical EMI and Crosstalk Topics:

Differential vs Common Mode Signals
Forward/Backward Crosstalk
Critical Length

Routing Over Slots in Planes
Routing Over Unrelated Planes
Routing Through Pin Fields

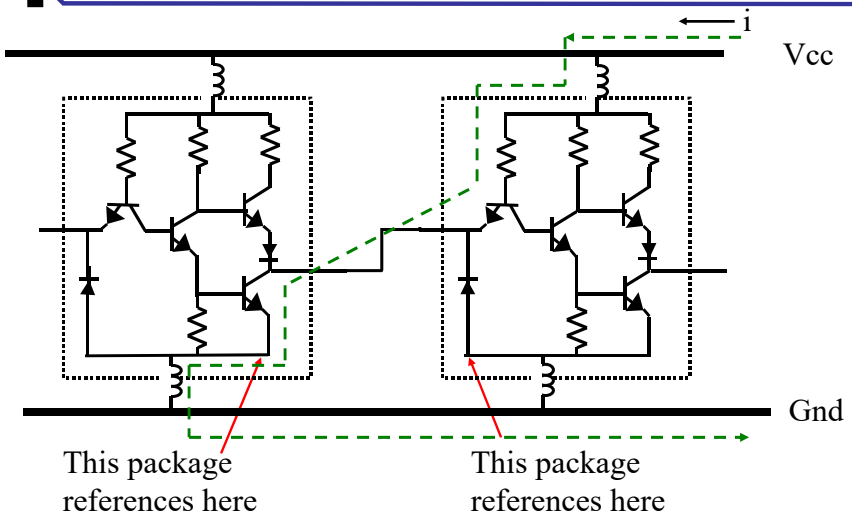
Primary Focus:
Minimize Loop Area.

Ground Bounce

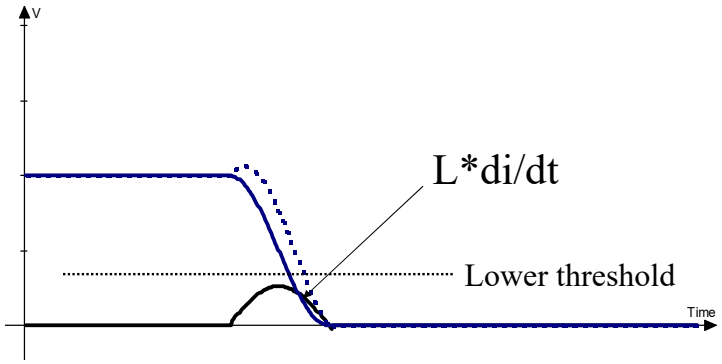


Two IC gates, but they are **NOT** connected here!

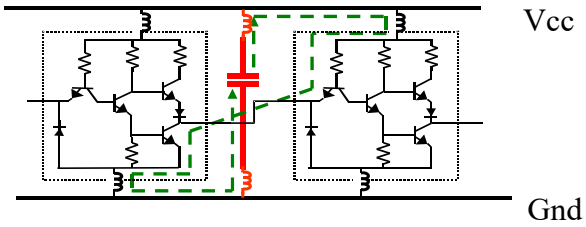
Ground Bounce



Ground Bounce



Ground Bounce

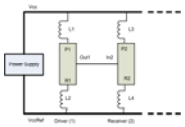


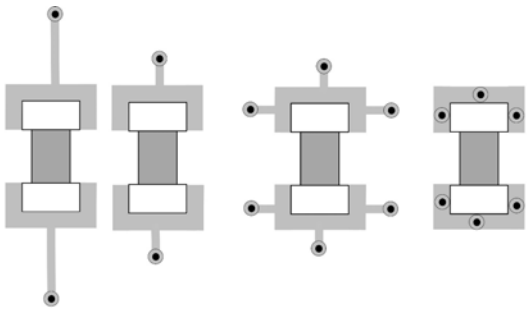
Solutions:

1. **Use bypass capacitors**
2. **Compensate for bypass capacitor inductance with planar capacitance.**
3. **Minimize inductance at pads**

See: Rick Hartley, *Controlling Radiated EMI Through PCB Stack-Up*, "Printed Circuit Design", July, 2000, p16

Minimizing Inductance





Ways to minimize pad inductance, from worst to best.

Ground Bounce

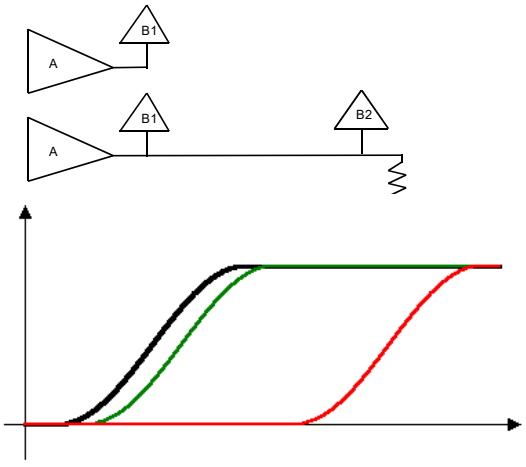
Typical Ground Bounce Topics:

Bypass Capacitors:
- **Size, How Many, Type and Placement**
- **Lead and Pad Inductance**
- **Self-Resonant Frequencies**
- **Bypass Capacitor ESR**

Low-inductance pads and connections
Planar Capacitance

Primary Objective:
- **Minimize Inductance**

Reflections



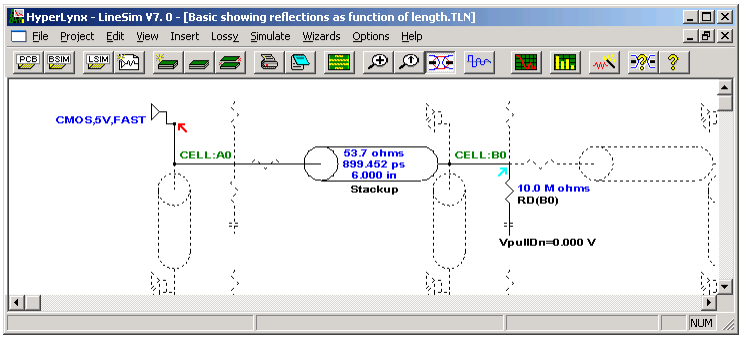
If Rise Time of driven signal (A) is 1 nanosecond:

And Tpd is 6"/ns
So one way critical length = 3"

Then (approx.)

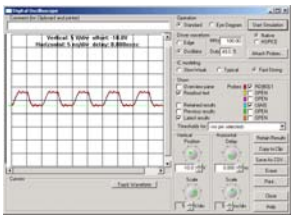
A - B1 = .3 ns = 1.8 in.
A - B2 = 2.2 ns = 13.2 in.

Reflections

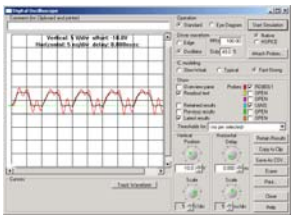


Simple HyperLynx Model
Rise time ≅ 1.6 ns
Critical length ≅ 3.3 inches
Open ended transmission line, length 2, 4, or 6”.

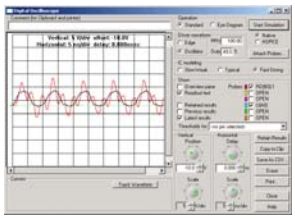
Reflections



2 in.

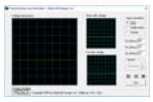


4 in.



6 in.

Trace length (relative to rise time) dictates severity of reflection



Reflections Solution

Make traces look like transmission lines
(Controlled impedance traces)

Terminate them in their characteristic impedance (Z_o)

Control impedance with geometry
(Height above *plane*, width, ε_r)

Concept of "*Critical Length*." (When the "round trip" propagation time is longer than the rise/fall time.)

Reflections Solution

Typical Reflection Topics:

- **Impedance (Depends on geometry)**
- **Terminations and their Placement**
- **"Y's"**
- **Stubs**
- **Vias**
- **Routing Over Slots in Planes**
- **Routing Over Unrelated Planes**
- **Routing Through Pin Fields**
- **Critical Lengths**
- **Differential Impedance**
- **Loop Areas**

Reflections Solution

Primary Objective:

Controlled Impedance
Terminations

Stage 2 Solutions

Route traces close to continuous, related planes
(Minimize loop area)

Control EMI
Control crosstalk
Control transmission line impedance

Use Power-Ground plane pairs (planar capacitance)

Control ground bounce
Control common-mode EMI

See: Rick Hartley, *Controlling Radiated EMI Through PCB Stack-Up*, "Printed Circuit Design", July, 2000, p16

Stage 3

Resistance = Fn(Frequency)

Traditionally:

L > 90º phase shift, presents a Z proportional to frequency
C > -90º phase shift, presents a Z inversely prop. to freq.
R > 0º phase shift, presents a Z independent of frequency

Stage 3

Causes:

Skin Effect: **Current density issue**
Related to inductance

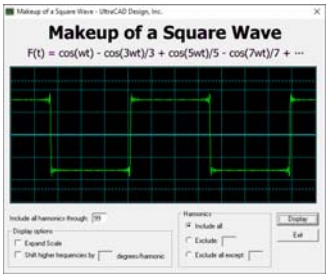
Dielectric Loss: **Molecular effect**

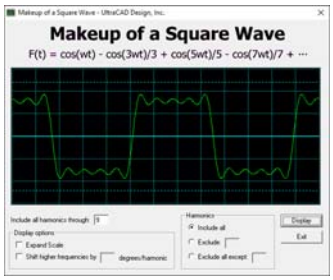
Manifestation:

Attenuation of higher frequency harmonics
“Lossy” transmission lines

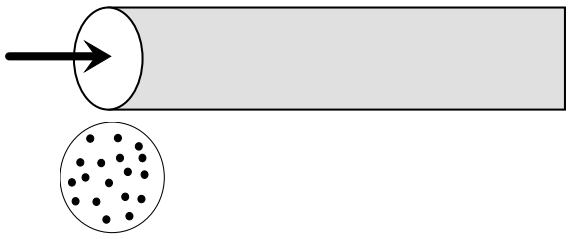
Stage 3 Manifestation

Attenuation of higher frequency harmonics results in a "Lossy" transmission line



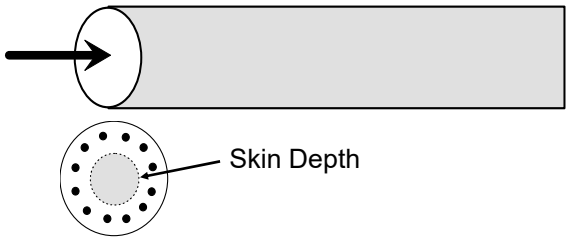


What is Skin Effect, 1



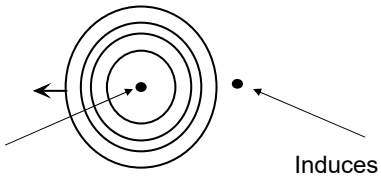
At "low" frequencies, current density is uniform across the cross-sectional surface of the conductor.

What is Skin Effect, 2



At "high" frequencies, current density is more concentrated around the outside edge of the cross-sectional surface of the conductor.

Cause of Skin Effect, 1



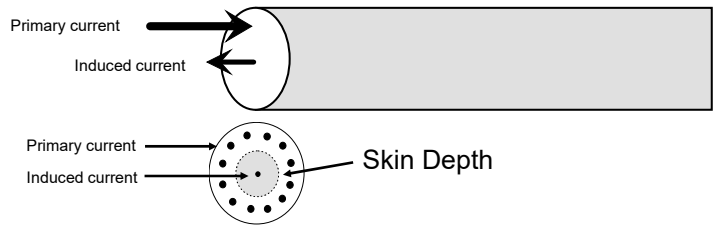
Increasing current flowing out of the page here…..

Induces a current flow into the page here

- A ***changing*** current in one wire causes a ***changing*** magnetic field (Ampere's Law) that induces a current in the opposite direction in an adjacent wire. (Faraday's law)

Principal behind a generator and a transformer!
Force behind EMI and cross talk!

Cause of Skin Effect, 2



THEREFORE: A *changing* current in one wire causes a *changing* magnetic field that induces a current in the opposite direction in *itself!*

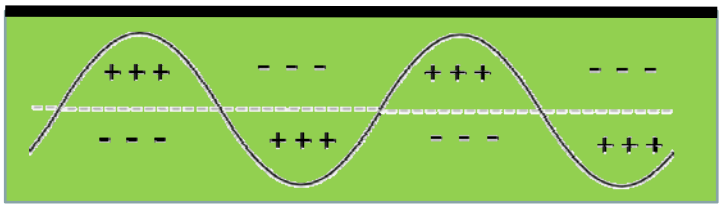
This is the basic nature of inductance

Skin Effect Result

The apparent resistance of the conductor increases:

1. ***NOT because the resistance of the conductor is changing,***
2. ***But because the current is flowing through a smaller cross-sectional area of the conductor.***

Dielectric Loss



As the signal moves down the trace, the charges alternately move from the top to the bottom of the dielectric and back again.

This motion requires energy to accomplish. That energy is absorbed from the waveform and represents an energy loss from the signal.

We can represent that energy loss as a resistor across the dielectric, and therefore the loss as an I^2R loss from the signal.

Equivalent Circuit

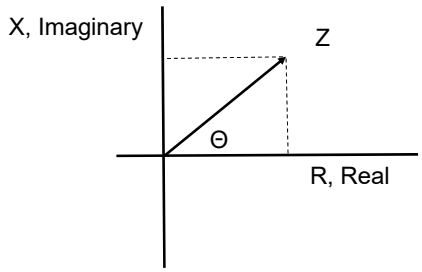
In the ideal case, R is ∞.

For a parallel RC circuit,

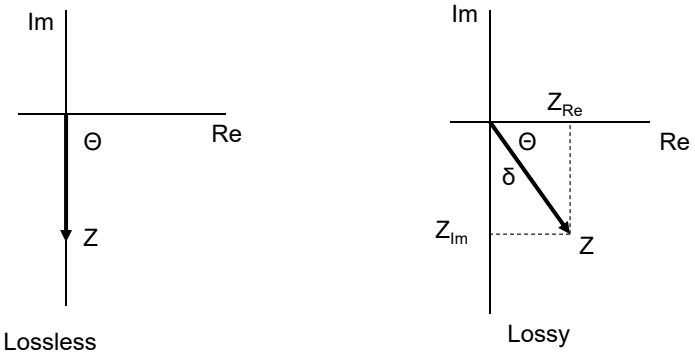
$$Z = \frac{1}{\frac{1}{X} + \frac{1}{R}} = \frac{1}{\frac{1}{1/j\omega C} + \frac{1}{R}}$$

Impedance

$$Z = R + jX$$



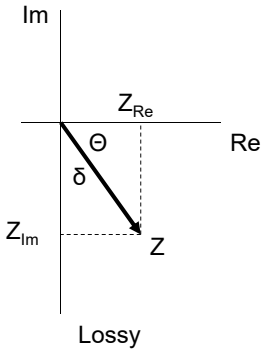
Impedance Diagram



Θ = Phase shift (-90 degrees in lossless situation)

δ = 90 - Θ = loss??

Loss Tangent



Tan(δ) = side opposite/side adjacent

$= Z_{Re} / Z_{Im}$

$= R/\omega R^2 C$

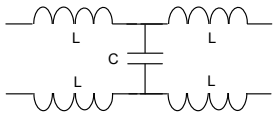
$= 1 / \omega RC$

$\omega = 2\pi f$

$\left.\begin{matrix} \mathrm{Tan}(\delta) \\ \mathrm{Tan(d)} \\ \mathrm{Tand} \end{matrix}\right\} = \mathrm{Loss\ \ Tangent}$

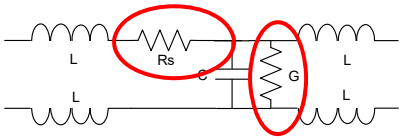
Stage 3 Practical Impact

Lossless transmission line:



$$Zo = \sqrt{\frac{L}{C}}$$

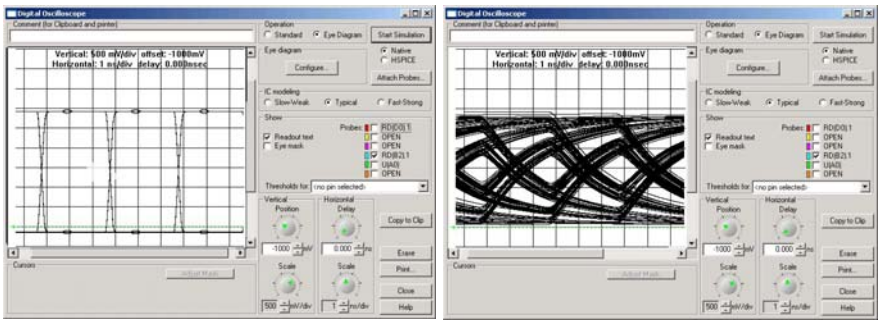
Lossy transmission line:



$$Zo = \sqrt{\frac{Rs + j\omega L}{G + j\omega C}}$$

G = conductance = 1/R

Stage 3 Eye Diagram



Lossless Lossy

Transmission line modeled with
Mentor Graphic's HyperLynx tool, v. 7

Stage 3 Solution

Equalization: **(Restore balance between harmonics)**

Active:

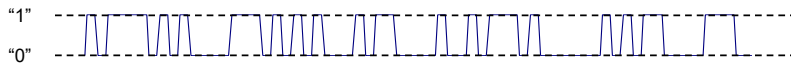
Do signal conditioning on the chip

Passive:

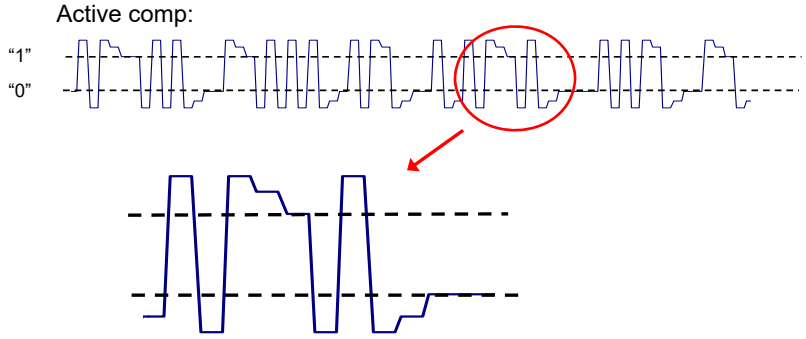
Add RC filter (equalization) to the transmission line

Active Signal Conditioning

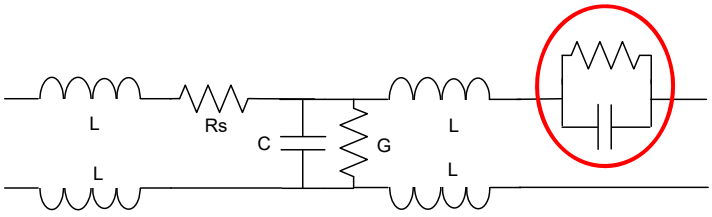
No comp:



Active comp:

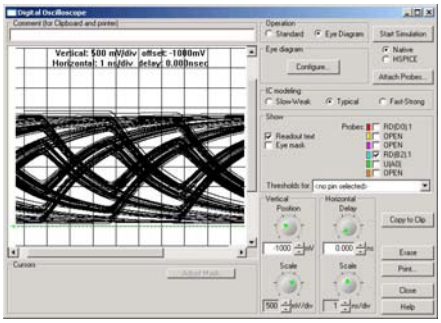


Passive (RC filter Equalization)

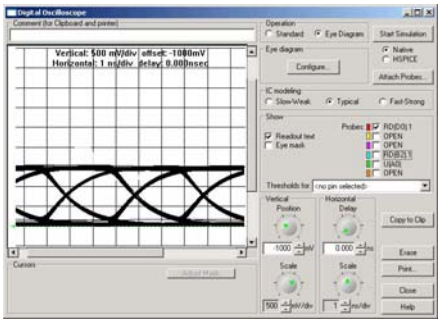


Parallel RC network compensates by passing the high frequency signals but attenuating the lower frequency ones.

Passive Equalization



Lossy simulation, without equalization



Lossy, with passive equalization

Stage 3 Solution

Equalization: **(Bring harmonics back into balance)**

Active vs Passive

Pre- vs Post-

Stage 4

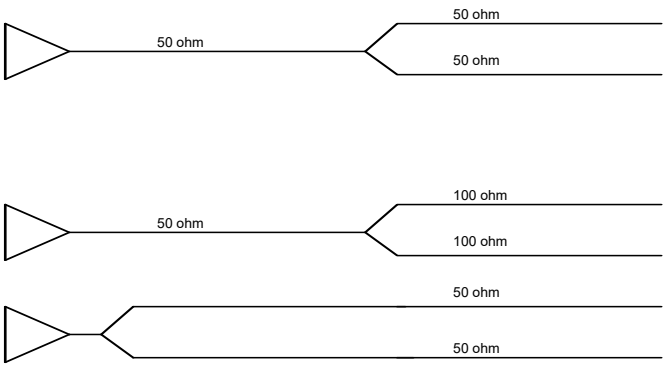
Transitions and Interconnections:

The ***critical length*** becomes so ***short*** we can no longer implement a solution.

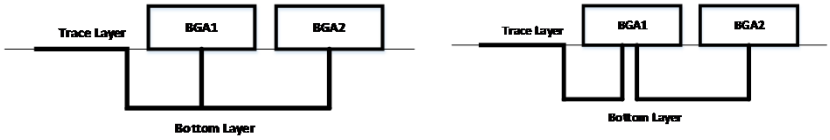
[at 100 ps rise time (≈ 3 GHz) critical length ≈ .25"]

Stage 4 Major Problem

Problem with "Y" connections:



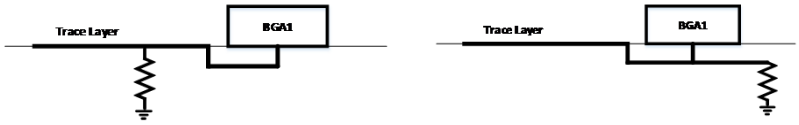
Some Solutions



a b

“a” is wrong, it creates a “Y”. “b” is better.

Problem With “Y” Stub



a b

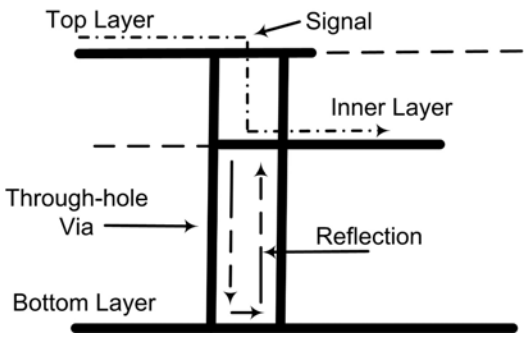
“a” is wrong, it creates an unterminated “Y” stub. “b” is better.

Stage 4 Solutions

Since:

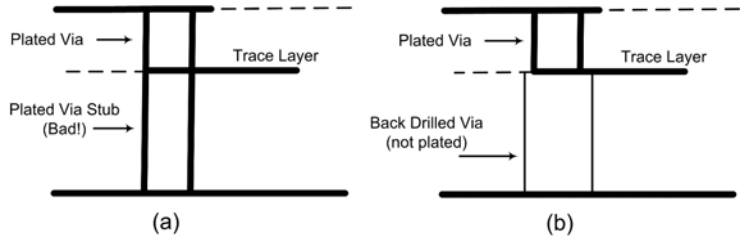
1. **We don't fully understand these problems,**
2. **We don't have an agreed set of solutions.**

Some Solutions



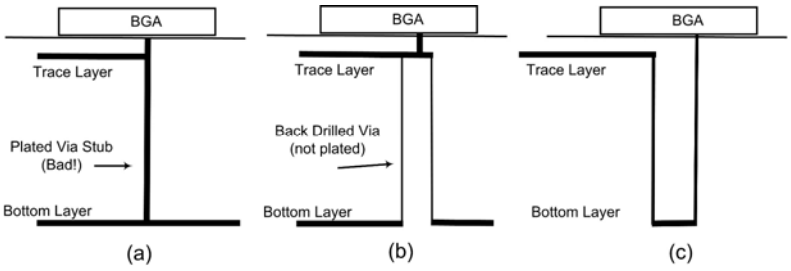
At very fast rise times, this reflection can matter!

Some Solutions



Eliminate reflection by back drilling.

Some Solutions



Alternative ways to access BGA pins.

Summary

Stage	Problems	Solutions
1	None	na
2	Inductance	Layout & Transmission Line
3	R = fn(F)	Equalization
4	Transitions & Interconnections	Layout

Thank You!

